



PCI-SIG PCI Express™ Frequently Asked Questions 7/24/02



Q1: What is PCI?

A1: PCI, or Peripheral Component Interconnect, is a parallel bus architecture developed in 1992 and is the predominant local bus designed in PCs and server platforms today. Over the years, the PCI-SIG has made numerous improvements to this technology and extended its application.

Q2: What is PCI Express?

A2: PCI Express is the official name for the architecture formerly known by the code name third generation I/O or 3GIO architecture. The name and its associated logo is a trademark of the PCI-SIG.

Q3: Why was PCI Express chosen as the name for this technology?

A3: The name reflects the high-speed, point-to-point qualities of the new architecture, and acknowledges that software compatibility is maintained between PCI and PCI Express.

Q4: What are the PCI Express 1.0 specifications and who developed them?

A4: The PCI Express 1.0 specifications are comprised of the core 'Base' and 'Card Electromechanical' specifications. The Base specification describes the protocol, signaling, software and other aspects of the technology while the Card Electromechanical specification describes the ATX-based form factors. The PCI Express specifications were developed by the Arapahoe Working Group (AWG) and transferred to the PCI-SIG with the approval of its Board of Directors. The specifications have been reviewed by the general membership of the PCI-SIG, ratified by the PCI-SIG Board of Directors and are now available worldwide for use in computing and communications platforms. These specifications will be maintained and enhanced by the PCI Express workgroup established in the PCI-SIG.

Q5: What is PCI Express architecture and why is it needed?

A5: The demands of emerging computing and communications platforms exceed the capabilities of the traditional PCI bus. Technical innovations such as 10 GHz+ CPU speeds, faster memory, high-performance graphics, gigabit networking, high-speed consumer devices and other market requirements will drive the need for much greater internal system bandwidth. The PCI Express architecture is a low-cost, highly scalable, general-purpose serial I/O interconnect that provides a unifying standard for consolidating a number of I/O solutions within a platform. For example, PCI Express can be used to replace the existing PCI, AGP and core logic interconnects. PCI Express provides:

- An open specification designed from the start to address the varying requirements of multiple market segments in both the computing and communications industries.
- Bandwidth scalability of up to 8 gigabytes per second. Future signaling improvements may provide even greater bandwidth headroom.
- Support for multiple widths, or as defined in serial architecture, multiple lanes (1, 2, 4, 8, 12, 16 and 32).
- Efficient, cost-effective, low pin-count interface offering maximum bandwidth per pin, and enabling small form factors.
- PCI compatibility through the established PCI software model (PCI enumeration, device driver, etc), providing a smooth transition to new hardware while allowing software to evolve to take advantage of new and extended PCI Express features.
- Support for add-in modules and plug-n-play capability.
- Support for many advanced RAS features, such as error handling and correction, aggressive power management, QoS, isochrony, native hot attach/detach, peer-to-peer support, etc.

Q6: What are the key features of the PCI Express technology?

A6: The key features of the PCI Express technology are:

- Compatibility with current PCI enumeration and software device driver models
- Layered architecture enabling physical layer attachment to copper, optical, or emerging physical signaling media to allow for future encoding schemes

PCI Express Frequently Asked Questions

- Maximum bandwidth per pin to enable unique and small form factors, simplify board design and routing, and reduce signal integrity issues
- Embedded clocking scheme enables extensive frequency scalability
- Bandwidth scalability with frequency and/or interconnect width
- Predictable low latency suitable for applications requiring isochronous data delivery
- Quality of Service (QoS) attributes
- Mechanisms to support embedded and communications applications
- Hot Plug and Hot Swap capability
- Power Management capabilities
- Extended configuration attributes
- Advanced peer-to-peer communication to support multi-hierarchy topologies

Q7: How does PCI Express enable new computer form factors? When will we see these new form factors in the market?

A7: PCI Express architecture's low signal-count links allow flexible I/O partitioning which enables split systems as well as end-user access to hot swappable PCI Express expansion modules. The PCI-SIG can not predict vendor product availability; however, new form factor concept designs are in development and we expect initial silicon and systems with new form factors to emerge beginning in 2H 2003.

Q8: How does the PCI Express deliver maximum bandwidth per pin? Why is this important?

A8: Serial technology overcomes the limitations of parallel bus architectures by delivering high bandwidth with the minimum number of signals. This allows higher frequency scaling, while maintaining cost effectiveness and easier routing in the design of printed circuit boards. For more information about the PCI Express architecture, visit <http://www.pcisig.com>.

Q9: When are PCI Express-based products expected?

A9: The PCI-SIG can not predict vendor product availability or comment on unannounced product plans of its member companies; however, some members have announced that they expect to have initial silicon based on the PCI Express architecture beginning in 2H 2003.

Q10: Is there a need for increased bandwidth? What are examples of this need?

A10: The demands of emerging computing and communications platforms exceed the capabilities of the traditional 32 bit, 33 MHz PCI bus. Technical innovations such as 10 GHz+ CPU speeds, faster memory, higher-speed graphics, gigabit networking, 1394b, and other applications will drive the need for much greater internal system bandwidth. For example, both 1394b and Gigabit Ethernet require bandwidth that exceeds PCI's current shared 133MB/sec maximum bandwidth. The PCI Express architecture is a high-speed, general-purpose serial I/O interconnect that provides the bandwidth required for current and future applications.

Q11: What is the difference between serial and parallel bus architecture?

A11: Serial technology delivers the necessary I/O bandwidth in the fewest number of signal pins. This allows a wide range of bandwidth scaling (in both width and frequency) while maintaining optimal cost effectiveness. Also, serial interconnects like PCI Express are free from the stringent synchronization requirements of parallel busses.

Q12: What is the difference between PCI Express and PCI-X 2.0? Is PCI Express intended to replace PCI-X?

A12: The PCI roadmap will continue to evolve well into the future. PCI will continue to be the flexible industry choice for chip-to-chip and add-in option devices. Both PCI Express and PCI-X 2.0 have key attributes that benefit the PCI-SIG members. PCI Express is a serial I/O interconnect while PCI-X 2.0 is a parallel bus. The PCI-SIG actively promotes both technologies as interfaces used in slots, adapter cards and in embedded devices.

PCI Express Frequently Asked Questions



Q13: Does this mean that PCI-X is going away?

A13: No. PCI-X will continue to be used in current and future applications as determined by our members and consistent with market requirements.

Q14: Will PCI Express slots co-exist with PCI or PCI-X?

A14: PCI Express slots can co-exist with PCI and PCI-X. Actual platform implementations will be determined by OEMs and IHVs.

Q15: Does PCI Express reside in-the-box or out-of-the-box?

A15: PCI Express is designed for 'in-the-box' applications. PCI Express can be used for chip-to-chip and add-in card applications to provide connectivity for adapter cards, as a graphics I/O attach point for increased graphics bandwidth, as well as an attach point to other interconnects like 1394b, USB 2.0, InfiniBand and Ethernet. PCI Express can also be used in embedded and communications applications.

Q16: Will PCI Express replace AGP?

A16: PCI Express is designed for use as a graphics I/O attach point. The initial graphics definition for PCI Express provides double the bandwidth of AGP8X. However, the PCI-SIG cannot predict whether its technologies will replace other technologies.

Q17: Is PCI Express intended to replace Serial ATA?

A17: PCI Express is not intended to replace Serial ATA. PCI Express and Serial ATA are complementary I/O interconnects that will co-exist. Serial ATA is dedicated to internal storage devices and is 100% software compatible with today's parallel ATA. This relationship is similar to how parallel ATA and PCI co-exist in today's platforms.

Q18: Does the PCI Express architecture compete with other I/O technologies such as HyperTransport or RapidIO?

A18: No. There are many technologies in the industry that have been developed to solve specific application needs. The PCI Express architecture is a general-purpose I/O interconnect optimized for connecting components within a platform. It retains PCI software compatibility while providing connectivity in chip-to-chip applications, I/O interconnect for adapter cards, I/O attach point to other interconnects like 1394b, USB2.0, InfiniBand and Ethernet, and as a graphics I/O attach point for next-generation graphics applications.

Q19: For what types of applications and systems will the PCI Express architecture be used?

A19: PCI Express architecture is designed from the ground up as a general-purpose I/O interconnect that can scale across multiple market segments in both the computing and communications industries. It is designed to provide connectivity as a chip-to-chip interconnect, I/O interconnect for adapter cards, an I/O attach point to other interconnects like 1394b, USB2.0, InfiniBand and Ethernet and as a graphics I/O attach point for increased graphics bandwidth.

Q20: Will the IP licensing model change for PCI Express compared with other PCI-SIG technologies?

A20: No. All PCI technologies are governed uniformly in accordance with the terms outlined in the PCI-SIG by-laws.

Q21: What changes did the PCI-SIG make to the PCI Express specifications based on the PCI-SIG membership review?

A21: One of the key benefits of PCI-SIG membership is the opportunity for a 60-day membership review of draft specifications prior to release. For the PCI Express membership review, member comments resulted in over 100 specification improvements. The PCI Express workgroup did not encounter any substantial technical issues or IP-related concerns during the membership review period.

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Q22: How much investment is required to integrate the PCI Express standard into a new or existing platform?

A22: We expect PCI Express technology to be at cost parity with PCI in volume production. As with any technology, there will be some investment necessary for product development and validation. Industry leaders recoup these costs fairly quickly as adoption rates increase.

Q23: How can I get a copy of the PCI Express specification?

A23: A benefit of membership in the PCI-SIG is access to both published specifications and draft specifications (see membership benefits at: http://www.pcisig.com/membership/about_us/). The specification is also available to non-members for a price. Current specifications can be obtained either through the PCI-SIG website: www.pcisig.com, or by calling 503-291-2569.